Listing of the Claims:

1. (Currently Amended) Trench isolation structure, comprising:

a slab of semiconducting material having a surface and a buried layer which extends parallel to the surface, the buried layer having an upper surface and a lower surface; and

a trench groove extending at least from the surface through the buried layer down to a part of the slab below the buried layer and

the trench groove including a liner of a first insulating material on and extending along a wall of the trench groove from above the upper surface to below the lower surface of the buried layer, and

wherein a remaining part of the trench groove is at least partially filled with a first filler material, and wherein the liner is characterized by an abrupt increase in thickness ~~,~~ in at least a first part of the trench groove that is substantially in line with ~~the upper and lower surfaces of~~ the buried layer, the abrupt increase in thickness defining ~~has~~ a thickness that is larger than a thickness of the liner in a second part of the trench groove, the second part of the trench groove located below the first part.

2. (Previously presented) Trench isolation structure according to claim 1, characterized in that the thickness of the liner in the first part of the trench groove is larger than a thickness of the liner in a third part of the trench groove, the third part of the trench groove located above the first part of the trench groove.

3. (Currently Amended) Trench isolation structure according to claim 1, characterized in that ~~the first part of~~ the trench groove is completely lined ~~filled~~ with the first insulating material.

4. (Previously presented) Trench isolation structure according to claim 3, characterized in that the first part of the trench groove extends substantially in line with the buried layer.

5. (Currently Amended) A ~~Semiconductor assembly, comprising a~~ trench isolation structure according to claim 1, wherein ~~and~~ at least one semiconductor device is at least partially present on the surface of the slab of semiconducting material, and wherein the semiconductor device is insulated by ~~means of~~ the trench isolation structure.

6. (Withdrawn) Method for forming a trench isolation in a semiconductor slab, comprising the steps of:

providing a slab of semiconducting material, having a first surface and comprising a buried layer parallel to and below the first surface, the buried layer having an upper surface and a lower surface;

forming a trench groove in the semiconductor slab, the trench groove having a bottom surface and a sidewall, and extending from the first surface through the buried layer and into the slab of semiconducting material;

filling the trench groove at least with a first insulating material and with a first filler material, wherein the first insulating material covers at least the bottom surface and the sidewall in a layer, and wherein the first filler material at least partially fills a remaining part of the trench groove,

characterized in that at least in a first part of the trench groove, the layer has a thickness that is substantially in line with the upper and lower surfaces of the buried layer and that is larger than a thickness of the layer in a second part of the trench groove, the second part of the trench groove located below the first part of the trench groove.

7. (Withdrawn) Method according to claim 6, characterized in that the thickness of the layer in the first part of the trench groove is made larger than ~~the~~ a thickness of the layer in a third part of the trench groove, the third part of the trench groove is located above the first part of the trench groove.

8. (Withdrawn) Method according to claim 6, characterized in that the step of filling the trench groove comprises the steps of:

covering the bottom surface and the sidewalls of the trench groove with a layer of first insulating material;

filling the trench groove with a first filler material at least to a lower surface level of the buried layer;

removing the first filler material down to a level which is substantially flush with the lower surface level of the buried layer; and

filling the remaining part of the trench groove at least partially with a second insulating material.

9. (Withdrawn) Method according to claim 8, characterized in that the step of filling the remaining part with the second insulating material is followed by the steps of removing the second insulating material down to a level which is substantially flush with an upper surface level of the buried layer, and filling the remaining part of the trench groove with a second filler material.

10. (Withdrawn) Method according to claim 8, characterized in that the step of removing the first filler material or of the second insulating material comprises etching the material.

11. (Cancelled).

12 . (New) A semiconductor structure providing trench isolation, the structure comprising:

a slab of semiconducting material having a surface and a buried layer which extends parallel to the surface;

a first insulating material;

a trench groove extending at least from the surface through the buried layer down to a part of the slab below the buried layer, the trench groove having a wall that is at least predominately lined and covered by the first insulating material from above an upper surface of the buried layer to below a lower surface of the buried layer, and the first

insulating material having a common thickness above and below the buried layer and having an increased thickness in at least part of the trench groove that is substantially in line with the buried layer; and

a first filler material at least partially filling a remaining part of the trench groove in areas above and below the buried layer.

13. (New) A semiconductor structure according to claim 12, characterized in that the increased thickness is defined by abrupt transitions respectively located near the upper surface of the buried layer and near the lower surface of the buried layer.

14. (New) A semiconductor structure according to claim 12, characterized in that the increased thickness is substantially in line with the buried layer.

15. (New) A semiconductor structure according to claim 12, characterized in that the part of the trench groove extends substantially in line with the buried layer.